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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/911,735	07/25/2001	Hideo Yoshida	1163-0349P	5603

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EXAMINER	
ABRAHAM, ESAW T	

ART UNIT	PAPER NUMBER
2133	4

DATE MAILED: 05/19/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

PRG

Office Action Summary	Application No. 09/911,735	Applicant(s) YOSHIDA ET AL.	
	Examiner Esaw T Abraham	Art Unit 2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 July 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 2.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims **1-24** are presented for examination.

Priority

2. Acknowledgment is made of applicant's claim for foreign priority under 35 U.S.C. 119(a)-(d).

Information Disclosure Statement

3. The examiner has been considered the references listed in the information disclosure statement submitted on 07/25/01.

Specification

4. The **title** of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

5. The **abstract** of the disclosure is objected to because the abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "means" and "said," should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details. The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc. Correction is required. See MPEP § 608.01(b).

6. The **disclosure** is objected to because of the following informalities:

a) Change the number "(39 in fig. 29)" to "(39 in fig. 20)" since there is no figure 29 (see page 1 paragraph 3 line 6).

(b) Change the number "(41 in fig. 2)" to "(41 in fig. 20)" (see page 1 paragraph 3 line 9). Correction of the following is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

7. Claims 2, and 8 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

a) Regarding to claims 2 and 8, the phrase "it is based on one error correction code parameter in data transmission" renders the claim indefinite because the phrase "wherein it is based on one error correction code parameter in data transmission" is not clear if the applicant is referring to the coded data, the sequence of data with the error correction or the check portion of the error correction code. The examiner would appreciate if the applicant would clarify this.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) The invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

8. Claims **1-24** are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Baggen et al. (U.S. PN: 5,872,798).

As per claim **1,** Baggen et al. teach or disclose an improvement data rate and a digital error protection when encoding and decoding (see col. 1, last paragraph). Beggen et al. teach that digital information signals are transferred in the form of a plurality of a number of sequences of information symbols whereby each information symbol has a uniform bit length and each sequence of information symbols occurs in a respective input channel. Further, Beggen et al. teach that check words are included in transmitted digital information signals and are encoded to allow correction of erroneous symbols caused on transmission (see abstract). Furthermore, Baggen et al. teach a method for transmitting an information signal in the form of sequences of information symbols, check symbols being included in the transmitted digital information signal as a result of encoding to enable correction of erroneous symbols caused by transmitting, said method comprising the steps of applying a first block of s symbols, one from each input channel of a plurality of input channels, in a first arranging state to a first error correcting encoder to generate p first check symbols and applying the resulting second block of symbols to a second error-correcting encoder to generate second check symbols, and transmitting said information symbols and said first and second check symbols (see claim 1).

As per claim **2,** Beggen et al. teach all the subject matter claimed in claim 1 including Beggen teach the method of applying a first block of symbols, one from each input channel of a plurality of input channels, in a first arranging state to a first error correcting encoder to generate p first check symbols; delaying each symbol in said first block and each of the p first check symbols by a respective different delay time to provide a resulting second block of

symbols in a second arranging state, each symbol of the resulting second block originating from a respective different first block; and applying the resulting second block of symbols to a second error-correcting encoder to generate q second check symbols, and transmitting said information symbols and said first and second check symbols, such that said first and second check symbols are generated to satisfy a respective parity check matrix (see claim 1)

As per claims **3 and 5,** Beggen et al. teach all the subject matter claimed in claim 1 including Beggen teach that a digital information signals are transferred in the form of a plurality of a number of sequences of information symbols whereby each information symbol has a uniform bit length and each sequence of information symbols occurs in a respective input channel. Further, Beggan teach the step of applying a third a fourth block of symbols dealing with the error-correcting decoders (see claim 3).

As per claim **4,** Beggen et al. teach all the subject matter claimed in claim 1 including Beggen teach the step of applying a first block of s symbols, one from each such input channel, in a first arranging state to a first error correcting encoder to generate p first check symbols (error detection) (see col. 1, lines 21-31). Further, Beggen et al. teach detecting of the block size can be done on the basis of a size indicator included in the block header (see col. 20, lines 4-7).

As per claim **6 and 7,** Beggen et al. teach decoding a digital information signal provided with error correction information by receiving a plurality of s+p+q sequence of input symbols, each symbol having a uniform bit length, and each such sequence of symbols occurring in a respective input channel, check words being included in the transmitted signal as a result of encoding to enable correction of erroneous symbols, said method further comprising the steps

of: applying a block of symbols, one from each input channel and in the first arrangement state, to an error-correcting decoder for decoding said block of symbols on the basis of p first check symbols; delaying each of the s user symbols and each of the q second check symbols in said block by a respective different delay time to provide a resulting (output) another block of symbols according to the second arranging state (see claim 3 and 8). Beggen et al. further teach that a method for decoding with error correction, to a device for transmitting with error protection, to a device for decoding with error correction, and to a carrier provided with information spaced, with respect to transmitting a finite sequence a trailing sequence of said first and second check symbols is generated by said delaying and retrocoupling and is limited to a series of s+q-1 first blocks comprising only notional information symbols (see col. 2, lines 16-65 and col. 3, 1-35).

As per claims **8-10,** Beggen et al. teach all the subject matter claimed in claim 6 including Beggen et al. teach a first error-correcting decoder for decoding a third block of symbols on the basis of p first check symbols; a second error-correcting decoder for decoding said fourth block of symbols on the basis of q second check symbols (see claim 3) and further Beggen et al. teach a step of executing after said decoding in said second error-correcting decoder of delaying all user symbols (see claim4).

As per claim **11,** Beggen et al. teach all the subject matter claimed in claim 6 including Beggen et al. teach decoding of a block code word can be achieved by combining decoders C1 and C2 (see figure 11) showing an (n-1+2m) * n matrix, the first n-1 columns at the left contain zeroes and are referred to the all-zero columns, the next m columns are called data columns.

Each data column comprises s data symbols in the s top rows and p+q parity symbols (error detection) in the p+q bottom rows (see col. 12, lines 17-53).

As per claims **12 and 13,** Beggen et al. teach all the subject matter claimed in claim 1 including Beggen et al. in figure 8 teach a block diagram of a decoding device that a stream of encoded symbols arrives at input (114) that is 8 bits wide for eight-bit symbols and after generating syndrome symbols, the decoder executes the decoding proper which may have various ones of the standard outcomes, find that the code word is correct and thus forego any correction, find certain errors correctable and correct them according to findings, or detect that the word is uncorrectable at least as far as the correction strategy goes (see col. 9, last paragraph).

As per claim **14,** Baggen et al. teach or disclose an improvement data rate and a digital error protection when encoding and decoding (see col. 1, last paragraph). Beggen et al. teach that digital information signals are transferred in the form of a plurality of a number of sequences of information symbols whereby each information symbol has a uniform bit length and each sequence of information symbols occurs in a respective input channel. Further, Beggen et al. teach that check words are included in transmitted digital information signals and are encoded to allow correction of erroneous symbols caused on transmission (see abstract). Furthermore, Baggen et al. teach a method for transmitting an information signal in the form of sequences of information symbols, check symbols being included in the transmitted digital information signal as a result of encoding to enable correction of erroneous symbols caused by transmitting, said method comprising the steps of applying a first block of s symbols, one from each input channel of a plurality of input channels, in a first arranging state to a first error

correcting encoder to generate p first check symbols and applying the resulting second block of symbols to a second error-correcting encoder to generate second check symbols, and transmitting said information symbols and said first and second check symbols (see claim 1).

As per claims **15 and 16,** Beggen et al. teach all the subject matter claimed in claim 1 including Beggen et al. teach that check words are included in transmitted digital information signals and are encoded to allow correction of erroneous symbols caused on transmission (see abstract). Although Beggen et al. do not teach soft determination decoding. However, this practice is deemed to be inherent to the error correction system of Beggen et al. because **by virtue of the fact** error-correction decoding section is commonly arranged to subject the composed signal to a soft determination decoding processing through use of the composed signal and the results of soft determination is

As per claims **17-19,** Beggen et al. in figure 1 teach a stream of data symbols arrives at input (100), a block (102) is the input storage that takes up the symbols according to order of arrival, and according to a selection mechanism that assigns the symbols to appropriate channels, a delay allows the various symbols to be presented to the first encoder stage (104) whereby the encoder (104) receive the incoming symbols at the same data rate as the input (100); for each data symbol received it determines the contribution thereby to the various first check symbols of the word of the first code to which the data symbol in question belongs and if necessary, it may calculate the contributions by the data symbols to check symbols of a cycle of first code words, block (106), an intermediate storage to align the data symbols and first check symbols for processing by a second encoder stage (108) and block (108) calculates in a similar way as the block 104, the second check symbols associated with the second code words and

block 110 is the output storage that takes up the data symbols and first and second check symbols for sequentially correct presentation to serial output 112 (see col. 5, lines 5-43 and claim 19).

As per claims **20-24,** Beggen et al. teach a device for decoding a digital information signal provided with error correction information comprising: input means comprising a plurality of input channels for receiving symbols according to a first arranging state, a first error-correcting decoder fed by said input means for decoding the symbols on the basis of first check symbols; a second error-correcting decoder fed by basis of second check symbols and for outputting at least the s decoder user symbols, such that each of said first and second error-correcting decoders is arranged to apply a parity check matrix of semi-cyclic codes (see claim 5). Further, Beggen et al. teach a delay means also applies the first check symbols after decoding, and puts adjacent symbols of said first arranging state into uniformly-spaced instances of said second arranging state, thereby executing an error protection operation in each of said first and second error-correcting decoder on both said first check symbols and said second check symbols, wherein for receiving a finite sequence of blocks stored according to a cylindrical format (see claim 5).

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

US PN: 6405338 Sinha et al.

US PN: 5706396 Schroder et al.

US PN: 5463641 Dorward et al.

US PN: 6675344 Sharma

US PN: 6370666 Lou et al.

US PN: 6012839 Nguyen et al.

10. Any inquiry concerning this communication or earlier communication from the examiner should be directed to Esaw Abraham whose telephone number is (703) 305-7743. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are successful, the examiner's supervisor, Albert DeCady can be reached on (703) 305-9595. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

Esaw Abraham

Esaw Abraham

Art unit: 2133

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